WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

an SRAM provided on a chip, the SRAM including an SRAM cell array;

a DRAM provided on the chip, the DRAM including a DRAM cell array; and

an address input circuit receiving an address signal, the address signal having a first portion and a second portion, the first portion carrying a unique value of row-column address information provided to access one of memory locations in one of the SRAM and DRAM cell arrays, the second portion carrying a unique value of SRAM/DRAM address information provided to select one of the SRAM and the DRAM.

2. The semiconductor memory device of claim 1, wherein the semiconductor memory device is configured with an SRAM bank and one or a plurality of DRAM banks, said SRAM constitutes a unit of the SRAM bank, and said DRAM constitutes a unit of each DRAM bank.

3. The semiconductor memory device of claim 1, wherein the semiconductor memory device is configured with a plurality of memory banks, and each memory bank contains both said SRAM and said DRAM as units of the memory bank.

4. The semiconductor memory device of claim 3, wherein said SRAM and said DRAM in one of the plurality of memory banks shares a column identifying circuit.

5. The semiconductor memory device of claim 4, wherein said shared circuit is a column decoder connected to each of the SRAM and DRAM cell arrays via sense amplifiers thereof.

6. The semiconductor memory device of claim 1, further comprising an address setting circuit for producing memory-select signals from the second portion of the address signal in response to mode-setting signals, the address setting circuit outputting the memory-select signals to the SRAM and the DRAM so as to access one of the SRAM and the DRAM, the memory-select signals carrying a unique value of secondary SRAM/DRAM address information that is changed from the SRAM/DRAM address information carried by the second portion of the address signal.

7. The semiconductor memory device of claim 1, further comprising a decoder, provided on the chip, for receiving the second portion of the address signal and for selecting one of the SRAM and the DRAM in response to the unique value of the SRAM/DRAM address information.

8. A semiconductor memory device comprising:

an SRAM memory block provided on a chip, the SRAM memory block including an SRAM cell array; and

a DRAM memory block provided on the chip, the DRAM memory block including a DRAM cell array,

wherein a source voltage is externally supplied to the DRAM memory block when the DRAM cell array is accessed, and said source voltage to the DRAM memory block is set to a ground voltage when the DRAM cell array is not accessed.

9. The semiconductor memory device of claim 8, further comprising:

a first power pad for receiving an SRAM source voltage, the SRAM source voltage being supplied from the first power pad to the SRAM memory block; and

a second power pad for receiving a DRAM source voltage, the DRAM source voltage being supplied from the second power pad to the DRAM memory block.

10. The semiconductor memory device of claim 8, further comprising:

a power pad shared by the SRAM memory block and the DRAM memory block, the power pad receiving the externally supplied source voltage; and

a control unit for controlling ON/OFF of the source voltage supplied from the power pad to the DRAM memory block in response to a control signal which is externally supplied to the control unit.

11. A semiconductor memory device comprising:

an SRAM memory block provided on a chip, the SRAM memory block including an SRAM cell array;

a DRAM memory block provided on the chip, the DRAM memory block including a DRAM cell array and an internal power supply circuit, the internal power supply circuit producing control voltages that are supplied to the DRAM memory block; and

a control unit for controlling the internal power supply circuit based on control signals that are externally supplied to the control unit, wherein, when the DRAM cell array is not accessed, the control unit controls the internal power supply circuit based on the control signals so that an operation of the internal power supply circuit is stopped and the control voltages are set in a predetermined condition.

12. The semiconductor memory device of claim 11, wherein the control signals, supplied to the control unit, include a DRAM activate control signal.

13. A semiconductor memory device comprising:

an SRAM memory block provided on a chip, the SRAM memory block including an SRAM cell array;

a DRAM memory block provided on the chip, the DRAM memory block having a DRAM cell array; and

a control unit connected to each of the SRAM memory block and the DRAM memory block, the control unit including a first pad and a second pad, the control unit activating an operation of one of the SRAM memory block or the DRAM memory block based on a combination of a first control value indicated by a first control signal presented to the first pad and

a second control value indicated by a second control signal presented to the second pad.

14. The semiconductor memory device of claim 13, wherein the first control signal is an SRAM enable signal and the second control signal is a DRAM enable signal, the control unit activating only the operation of the DRAM memory block when the SRAM enable signal is set at a low level and the DRAM enable signal is set at a high level, and the control unit activating only the operation of the SRAM memory block when the SRAM enable signal is set at a high level and the DRAM enable signal is set at a low level.

15. A semiconductor memory device comprising:

an SRAM memory block provided on a chip, the SRAM memory block including an SRAM cell array having bit lines connected to column switches, the column switches connected to a data bus;

a DRAM memory block provided on the chip, the DRAM memory block including a DRAM cell array, sense amplifiers and column gates, the DRAM cell array having bit lines connected to the column gates, the column gates connected to the data bus; and

column select signals provided to the column gates in order to select which sense amplifier output to connect to the data bus,

wherein, when accessing the SRAM cell array during a refresh operation of the DRAM cell array, all the column select signals are set to OFF state so that all the column gates are turned off by the column select signals.

16. The semiconductor memory device of claim 15, further comprising:

a first data bus switch provided between the data bus and the column switches of the SRAM memory block; and

a second data bus switch provided between the data bus and the column gates of the DRAM memory block,

wherein a DRAM/SRAM select signal is provided to both the first data bus switch and the second data bus switch so that the first and second data bus switches are turned on or off by the DRAM/SRAM select signal, and

wherein, when accessing the SRAM cell array during a refresh operation of the DRAM cell array, the first data bus switch is turned on and the second data bus is turned off by the DRAM/SRAM select signal.